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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,913	LAI ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/18/01; 2/11/02; 8/30/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/11/02* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/11/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-48 are examined.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: reference numbers cited in specification for Figure 1, 6, and 7 are not found in the drawings. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

There is no description for Figures 1A-1C, 6A-6B, 7A-7B, and 14-23 in the brief description and detail description.

Appropriate correction is required.

Claim Objections

4. Claims 10, 27, 33-39, 42-43, and 48 are objected to because of the following informalities:

Re claim 10, the phrase "the despreader/correlator unit" should re-write as "the despreader or correlator unit".

Re claim 27, the claim limitation is written incomplete which would not be understandable.

Re claims 33-39 and 42-43, these claims have same limitations cited in claims 18, 24-26, and 29-30. Therefore, the applicant is advised to remove these claims in order to avoid duplicated claims in the application.

Re claim 48, the phrase "unit units" should replace with "unit" for clarification. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7, 9-10, 14, 28-29, 32, 42, and 46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 7, the limitation "the instruction" in line 1 lacks an antecedence basis. For examination purposes, the examiner considers the instruction as an instruction.

Re claim 9, the term "can be" in 2 is a relative term which renders the claim indefinite. The term "can be" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For examination purposes, the examiner disregards the term. Claim 28 has the same problem.

Re claim 10, claim is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the function and relationship of the despreader/correlator unit and the structure of reconfigurable chip. For examination purposes, the examiner disregards this limitation. Claims 29 and 42 have the same problem.

Re claim 14, claim is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relationship of a state machine and the structure of reconfigurable chip. For examination purposes, the examiner disregards this limitation. Claims 32 and 46 have the same problem.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-48 are rejected under 35 U.S.C. 102(b) as being anticipated by D'Luna et al. (U.S. 5,311,459).

Re claim 1, D'Luna et al. disclose in Figures 1-6 a reconfigurable chip (e.g. reconfigurable to be a sequential matrix multiplier, a parallel matrix multiplier, a convolver, or a FIR fitler...) comprising: a multiplication block (e.g. Figure 2) including at least one multiplication unit (three multiplication units in Figure 2) and a group of selectable adder units (e.g. A1) operable connected to the multiplication unit (output of multiplication units connect to A1, wherein the adder units are selectively connectable in different configurations (configurable by B1 in the Mode_Select); and interconnect elements (e.g. Figure 3) operable connected to the multiplication block, the interconnect elements adapted to selectively connect together the multiplication block with other reconfigurable units (there are three units of multiplication block in Figure 3).

Re claim 2, D'Luna et al. further disclose in Figures 1-6 the multiplication block further comprises input multiplication multiplexers for the block (e.g. M1-M3 in Figure 2).

Re claim 3, D'Luna et al. further disclose in Figures 1-6 there are fewer block input multiplexers than input multiplexers for the multiplication units (e.g. there is only one multiplexer 29 in Figure 6 and there are three multiplexers for the multiplication units in Figure 2).

Re claim 4, D'Luna et al. further disclose in Figures 1-6 the adder units include input multiplexers (e.g. offset multiplexer in Figure 2).

Re claim 5, D'Luna et al. further disclose in Figures 1-6 the multiplication units include input multiplexers (e.g. M1-M3).

Re claim 6, D'Luna et al. further disclose in Figures 1-6 there are multiple multiplication units in each block (there are three multiplication units in the block as seen in Figure 2).

Re claim 7, D'Luna et al. further disclose in Figures 1-6 the instruction configures the multiplexers in the multiplication block (e.g. Mode_select instruction).

Re claim 8, D'Luna et al. further disclose in Figures 1-6 the multiplication block includes registers (e.g. Cx and Bx in Figure 2) associated with the multiplication unit and adder units.

Re claim 9, D'Luna et al. further disclose in Figures 1-6 the other type of unit is operable connectable to the adder units and can be used instead of multiplier units (e.g. Figure 3).

Re claim 10, D'Luna et al. further disclose in Figures 1-6 the other type of unit comprises the despreader/correlator unit.

Re claim 11, D'Luna et al. further disclose in Figures 1-6 the adder units can be connected together into chains (e.g. Figure 1).

Re claim 12, D'Luna et al. further disclose in Figures 1-6 the interconnect elements are adapted to transfer word length data (e.g. Figure 1 with input data router 12).

Re claim 13, D'Luna et al. further disclose in Figures 1-6 an instruction memory storing multiple instructions for the reconfigurable functional units (e.g. col. 4 lines 35-43).

Re claim 14, D'Luna et al. further disclose in Figures 1-6 a state machine addresses the instruction memory.

Re claim 15, D'Luna et al. further disclose in Figures 1-6 the multiplication 2 block includes a selectable output register for the multiplier units (e.g. Bx in Figure 2) and the adder units (e.g. OBI in Figure 2).

Re claim 16, D'Luna et al. further disclose in Figures 1-6 the multiplication block includes at least two multiplication units (there are three multiplication units in Figure 2).

Re claim 17, D'Luna et al. further disclose in Figures 1-6 the multiplication block includes at least four multiplication units (e.g. similar configuration in Figure 2 wherein there is no unity in expression 2).

Re claim 18, D'Luna et al. disclose in Figures 1-6 a reconfigurable chip (abstract) including: a multiplication block (e.g. Figure 2) including at least one input multiplexer (M1-M3), a multiplication unit (three multiplication in the middle portion of Figure 2) operably connected to the input multiplexer (M1-M3), a group of selectable adder units (A1-A3 in Figure 3) operably connected to the multiplication unit (Figure 2), wherein the adder units are selectively connectable in different manners (by the Mode_select through B1); and an instruction memory storing multiple instructions for the multiplication block (e.g. Mode_Select command).

Re claim 19, it has the similar limitations as cited in claim 2. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 20, it has the similar limitations as cited in claim 4. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 21, it has the similar limitations as cited in claim 5. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 22, it has the similar limitations as cited in claim 3. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 23, it has the similar limitations as cited in claim 6. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 24, it has the similar limitations as cited in claim 17. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 17.

Re claim 25, D'Luna et al. further inherently disclose in Figures 1-6 the multiplication block includes a decoder to decode a portion of the instruction (there must be an instruction to configure automatically or manually by setting the Mode_select and the instruction must be decode in a form for the machine to understand).

Re claim 26, it has the similar limitations as cited in claim 8. Thus, claim 26 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 27, D'Luna et al. further disclose in Figures 1-6 the registers of selectable output registers.

Re claim 28, it has the similar limitations as cited in claim 9. Thus, claim 28 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 29, it has the similar limitations as cited in claim 10. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 30, it has the similar limitations as cited in claim 11. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 31, D'Luna et al. further disclose in Figures 1-6 interconnect units operably connected to the multiplication block (Figure 3).

Re claim 32, it has the similar limitations as cited in claim 14. Thus, claim 32 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

Re claim 33, it has the same limitations as cited in claim 18. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 18.

Re claim 34, it has the same limitations as cited in claim 22. Thus, claim 34 is also rejected under the same rationale as cited in the rejection of rejected claim 22.

Re claim 35, it has the same limitations as cited in claim 24. Thus, claim 35 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 36, it has the same limitations as cited in claim 24. Thus, claim 36 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 37, it has the same limitations as cited in claim 18. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 18.

Re claim 38, it has the same limitations as cited in claim 25. Thus, claim 38 is also rejected under the same rationale as cited in the rejection of rejected claim 25.

Re claim 39, it has the same limitations as cited in claim 26. Thus, claim 39 is also rejected under the same rationale as cited in the rejection of rejected claim 26.

Re claim 40, D'Luna et al. further disclose in Figures 1-6 the registers are selectable output registers.

Re claim 41, D'Luna et al. further disclose in Figures 1-6 there is another type of unit operable connected to the adder units strictly used instead of the multiplier unit (e.g. 20 in Figure 2)

Re claim 42, it has the same limitations as cited in claim 29. Thus, claim 42 is also rejected under the same rationale as cited in the rejection of rejected claim 29.

Re claim 43, it has the same limitations as cited in claim 30. Thus, claim 43 is also rejected under the same rationale as cited in the rejection of rejected claim 30.

Re claim 44, it has similar limitations as cited in claim 12. Thus, claim 44 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 45, it has similar limitations as cited in claim 13. Thus, claim 45 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 46, it has similar limitations as cited in claim 32. Thus, claim 46 is also rejected under the same rationale as cited in the rejection of rejected claim 32.

Re claim 47, D'Luna et al. disclose in Figures 1-6 a multiplication block on a reconfigurable chip, the multiplication block (abstract) including: multiple block input multiplexers (e.g. the first block has M1-M3 in Figure 2); at least two multiplication units (there are three multiplication units in Figure 2), each multiplication unit associated with two multiplication input multiplexers (e.g. one from M1-M3 and other from 29 in Figure 6), the multiplication input multiplexers operably connected to the multiple block input multiplexers (e.g. 12 in Figure 2); and a group of selectable adder units (e.g. A1-A3 in

Figure 3) with associated adder input multiplexers, the adder input multiplexers operably connected to the multiplication units (e.g. add all the output of multiplication units).

Re claim 48, D'Luna et al. disclose in Figures 1-6 reconfigurable chip comprising: a multiplication block (e.g. Figure 2) including at least one multiplication unit (there are three multiplication units) and a group of selectable adder units (e.g. A1-A3 in Figure 3) operably connected to the multiplication unit (adder is used to add all the output of multiplication units), wherein the adder units are selectively connectable in different configurations (by the Mode_Select control into 15 in Figure 2); and reconfigurable functional units (15) operably connectable to the multiplication block, the reconfigurable functional units including an arithmetic logic unit and a shifter unit.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,530,010 to Hung et al. disclose a multiplexer reconfigurable image processing peripheral having for loop control.

b. U.S. Patent No. 6,212,618 to Roussel discloses an apparatus and method for performing multi-dimensional computations based on itra-add operation.

c. U.S. Patent No. 5,600,584 to Schlafly discloses an interactive formula compiler and range estimator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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August 3, 2004

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